Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-43. (canceled)

44. (currently amended) A semiconductor device, comprising:

a semiconductor chip including an inner circuit, an input pad, and a wiring ~~for connecting~~ that connects the input pad to the inner circuit;

a plurality of electrostatic protection elements connected to the wiring between the input pad and the inner circuit, each electrostatic protection element including ~~two~~ a pair of transistors ~~each of which forms part of a respective capacitor~~; and

a fuse disposed between the wiring and at least one of the electrostatic protection elements so that the fuse is between the at least one electrostatic protection element and the inner circuit, the fuse being selectively disconnectable so as to selectively disconnect the at least one electrostatic protection element from wiring when more than one semiconductor chip is mounted in a package with the semiconductor chip and commonly connected to the input pad.

45. (previously presented) The semiconductor device according to claim 44, wherein said electrostatic protection elements include a first electrostatic protection element and a second electrostatic protection element, said fuse being disposed

between the wiring and the second electrostatic protection element.

46. (previously presented) The semiconductor device according to claim 44, wherein said semiconductor chip includes a first semiconductor chip having a first wiring and a second semiconductor chip having a second wiring, said electrostatic protection elements respectively connected to the first wiring and the second wiring include a first electrostatic protection element and a second electrostatic protection element, and said fuse includes a first fuse and a second fuse, said first fuse being disposed between the first wiring and the second electrostatic protection element, said second fuse being disposed between the second wiring and the second electrostatic protection element so that the first fuse and second fuse are electrically disconnected.

47. (previously presented) The semiconductor device according to claim 44, wherein said semiconductor chip includes a first semiconductor chip having a first wiring and a second semiconductor chip having a second wiring, said electrostatic protection elements respectively connected to the first wiring and the second wiring include a first electrostatic protection element and a second electrostatic protection element, and said fuse includes first fuses and second fuses, said first fuses being disposed between the first wiring and the first electrostatic protection element and between the second wiring and the first electrostatic protection element, said second fuses being disposed between the first wiring and the second electrostatic protection element and the second wiring and the

second electrostatic protection element so that at least ones of said first fuses and said second fuses being electrically disconnected.

48. (previously presented) The semiconductor device according to claim 44, wherein said semiconductor chip includes semiconductor chips in a number of n each having the wiring wherein n is an integer more than 3; said electrostatic protection elements respectively connected to the wirings includes first to n-th electrostatic protection elements; and said fuse includes second to n-th fuses respectively disposed between the wirings and the second to n-th electrostatic protection elements so that the second to n-th fuses are electrically disconnected.

49. (currently amended) The semiconductor device according to claim 44, wherein said semiconductor chip includes semiconductor chips in a number of n each having the wiring wherein n is an integer more than 3; said electrostatic protection elements respectively connected to the wirings includes first to n-th electrostatic protection elements; and said fuse includes first to n-th fuses respectively disposed between the wirings and the first to n-th electrostatic protection elements so that at least one of the first to n-th fuses ~~being~~ are electrically connected.

50. (previously presented) The semiconductor device according to claim 44, wherein said semiconductor chip includes semiconductor chips in a number of n each having the wiring wherein n is an integer more than 3; said electrostatic

protection elements respectively connected to the wirings includes first to n-th electrostatic protection elements; and said fuse includes first to n-th fuses respectively disposed between the wirings and the first to n-th electrostatic protection elements so that at least two of the first to n-th fuses are electrically connected.

51. (previously presented) The semiconductor device according to claim 44, wherein said semiconductor chip includes semiconductor chips in a number of o or p each having the wiring wherein o and p are integers more than 2; said electrostatic protection elements respectively connected to the wirings includes a first to m-th electrostatic protection elements wherein m is a lowest common multiple of o and p; and said fuse includes second to m-th fuses respectively disposed between the wirings and the second to m-th electrostatic protection elements so that the (m/o + 1)-th to m-th fuses are electrically disconnected when the semiconductor chips are in the number of o, and the (m/p + 1)-th to m-th fuses are electrically disconnected when the semiconductor chips are in the number of p.

52. (previously presented) The semiconductor device according to claim 44, wherein said semiconductor chip includes semiconductor chips in a number of o or p each having the wiring wherein o and p are integers more than 2; said electrostatic protection elements respectively connected to the wirings includes a first to m-th electrostatic protection elements wherein m is a lowest common multiple of o and p; and said fuse includes first to m-th fuses respectively disposed between the wirings and the first to m-th electrostatic protection elements

disconnected when the semiconductor chips are in the number of o, and the (m/p + 1)-th to m-th fuses are electrically disconnected when the semiconductor chips are in the number of p.

53. (previously presented) The semiconductor device according to claim 44, wherein each of said electrostatic protection elements includes a P-channel transistor and an N-channel transistor.

54. (previously presented) The semiconductor device according to claim 44, wherein each of said electrostatic protection elements includes a grounding portion connected to ground.

55. (previously presented) The semiconductor device according to claim 53, wherein at least one of said P-channel transistor and said N-channel transistor is connected to ground.

56. (canceled)

57. (currently amended) A device, comprising:

a ~~plurality~~ pair of semiconductor chips, each semiconductor chip including an inner circuit, an input pad, and a wiring ~~for connecting~~ that connects the input pad to the inner circuit;

~~a plurality of electrostatic protection elements connected to the wiring between the input pad and the inner circuit, each electrostatic protection element including two transistors each of which forms part of a respective capacitor; and~~

~~a fuse disposed between the wiring and at least one of the electrostatic protection elements,~~

a first electrostatic protection element connected to the wiring at a first location between the input pad and the inner circuit;

a second electrostatic protection element selectively connected to the wiring at a second location, between the input pad and the inner circuit, downstream of the first location and the first electrostatic protection element; and

a pair of fuses respectively disposed between the wiring and different portions of the second electrostatic protection element so that the fuses are between the second electrostatic protection element and the inner circuit, the fuses being selectively disconnectable so as to selectively disconnect the second electrostatic protection element from the wiring,

wherein the input pads of the respective semiconductor chips are commonly connected to a common terminal.